Division of Electrical Engineering and Computer Science	Research field	VLSI Systems	Lab. ID EC08	
Laboratory web site	http://mics.w3.kanazawa-u.ac.jp/			
Research subjects				

Recently, most functions of multimedia information and communication system, represented by a smartphone, has been realized on a small silicon chip. The VLSI becomes a key technology to expand ICT industry. The miniaturization level enters in nano meter era, and the effective utilization of enormous hardware resources becomes the most important problem. This laboratory researches about the technologies to realize large integrated systems mainly for image processing, including VLSI architecture, circuit design technique, and design methodology. The main themes are 1) VLSI image processing, 2) VLSI image recognition, 3) high-performance memory with advanced functionality.

Master/Doctor course: Education policy, curriculum, typical activity in the laboratory

At the assignment to the laboratory, an interview is held to decide a study theme and a research group. There is a reading society by all members of the laboratory. In the society, an expert text is read. A member in turn explains the contents, followed by discussion. There are study sessions and progress meetings for each research group. In the study session, basic knowledges necessary for research are acuquired. In the progress meeting, each member in the group presents his or her experimental results, considerations, and future works. A member in this laboratory performs one or more external presentations by graduation. Almost all members join a company of the manufacturing industry after graduation.

Daily life in the laboratory, etc.

All the members basically exist in the laboratory from 10:00 to 17:00 except holidays. Other than the time for seminar and lecture, the activity in the laboratory is free. A desk is assigned to each member and are usable freely.

Message or comments by the laboratory faculty staffs

Think and act by oneself. Self-administration is strongly demanded so that you don't become lazy. Be careful with limited precious time.

Recent Master theses in these 3 years (+ more if appropriate)				
year.month	Thesis title (including English translation of Japanese thesis title)			
2020.3	FPGA implementation of low-bit quantized DNN for semantic segmentation			
2016.3	Development of a Disparity Estimation Algorithm using Superpixels			
2016.3	An Object Detection Processor using Statistics of Gradient Images as Image Features			
2016.3	Fast Pedestrian Detection using Statistics of Gradient Images as Image Features			
2014.3	Vehicle Detection and Tracking with Stereo Motion Segmentation			
2014.3	Development of Real-time Head Pose Estimation System			
2013.3	Depth Image Generation for Body Posture Estimation with Stereo Motion Segmentation			
Recent Doctoral theses in these 3 years (+ more if appropriate)				
year.month Thesis title (including English translation of Japanese thesis title)				
Laboratory mail address		MIYAMA,Masayuki <miyama *at*="" se.kanazawa-u.ac.jp=""></miyama>		